Amendments to the Specification:

In the SUMMARY OF THE INVENTION,
please replace the first full paragraph beginning at page 5 with the following amended paragraph:

As described in the referenced patent application (US Serial No. 10/764920), within a set of small capacitors, one capacitor after the other is switched in parallel to change the total sum of capacitance. To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance). To achieve said sliding switch operation, a typical implementation uses FET-transistors, one per capacitor. The switching operation of such FET-transistor can be divided into three phases: the fully-switched-off phase (RDS is very high), a steady ramp-up/ramp-down phase or steady transition phase and the fully-switched-on phase (RDS is very low). By thoroughly controlling such switching device within said steady ramp-up/ramp-down phase, the capacitor in series with said switching device is ~~effectively~~ partially switched in parallel with a well-controlled proportion between 0 % and 100 %.

Please replace the 3rd full paragraph beginning at page 6 with the following amended paragraph:

Additional circuit elements, described in the related US Patent Application, Serial No. 10/676919, filed Oct. 1, 2003, ~~and~~ titled "Translinear Amplifier" and hereby incorporated by reference, implement a signal-limiting function and provide a signal to sharply cut off said translinear amplifier's linear operation, once the defined linear operating range is exceeded at the negative end of said linear operating range; and to

sharply limit said translinear amplifier's linear operation, once the linear operating range

is exceeded at the positive end of said linear operating range. The circuits of said

signal limiting functions then either overdrives said switching transistor either into deep

saturation (RDSon going to 0) or overdrives it into its extreme off state (RDSoff going

very high) when said switching device is outside its desired steady transition phase.

Please replace three paragraphs, beginning with the 2nd 4th full paragraph at page 7
with the following three amended paragraphs:

The total concept according to the proposed invention is shown in **Fig. 6**. One

key point of the invention is the implementation of a-signal-limiting functions at both

ends of the steady ramp-up/ramp-down phase. Once the signal controlling the switching

device leaves the steady transition phase, the signal condition is changed abrupt. **Fig.**

7 visualizes this effect. The purpose is to drive said switching device to a fully-on state,

when said switching device is outside its steady transition phase on the lower resistance

side (low RDSon) and to drive said switching device to a fully-off status, when said

switching device is beyond its steady transition phase on the higher resistance side

(high RDSon).

Depending on the technique to implement the reference values for each of the

amplifiers within a chain of said translinear amplifiers-chain, even specific nonlinear

relations of capacitance change versus tuning voltage can be constructed.

The amplifier primarily generating the control signal for the switching devices is,

according to the invention, a translinear amplifier,as described in patent application, US

Serial No. 10/676919, filed Oct. 1, 2003. In addition, a-signal-limiting functions, which is

are designed to drive said switching device to a fully-on status, when said switching

device is outside its steady transition phase on the lower resistance side (low RDSon)

or to drive said switching device to a fully-off status, when said switching device is

outside its steady transition phase on the higher resistance side (high RDSon), can be

implemented. Such signal-limiting functions could, according to the invention, be

implemented with additional circuit elements within the translinear amplifier. It They

could however be implemented as separate circuits as well.

Please replace the 2nd full paragraph beginning at page 9 with the following amended
paragraph:

A translinear amplifier typically has a gain of 1. However, a gain different from 1

is also achievable, which, if implemented, gives one more degree of freedom in

dimensioning the circuit and optimizing certain operating parameters. For example, the

remaining overlapping of neighboring capacitor switching stages may be even further

reduced, as the slope of the steady ramp-up/ramp-down operation can be controlled

with adequate selection of the gain.

Please delete the first full paragraph beginning at page 11:

Even more, with a translinear amplifier with a gain different from 1, the whole

concept gains one more degree of freedom in optimizing certain operating parameters,

like the overlapping of neighboring switching stages.

In the DESCRIPTION OF THE PREFERRED EMBODIMENTS,
please replace five paragraphs, starting at the 1st paragraph beginning at page 15 with
the following five amended paragraphs

As described in said related patent application US Serial No. 10/764920, within a set of small capacitors **Cap 1** to **Cap n**, one capacitor after the other is switched in parallel to change the total capacity. Each capacitor has its individual switching device **Sw 1** to **Sw n.** To achieve a linear capacitance change, said capacitors are not switched on one by one in digital steps, however each capacitor is switched on partially in a sliding operation, starting at low value (0 % of its capacitance) and ending with the fully switched on capacitor (100 % of its capacitance). To achieve said sliding switch operation, a typical implementation uses FET-transistors, one per capacitor. The switching operation of such FET-transistor can be divided into three phases: the fully-switched-off phase (the FET's RDS is very high), a steady ramp-up/ramp-down phase or steady transition phase, where the series resistance of said FET-transistor steadily changes from high to low values or vice versa, and the fully-switched-on phase (the FET's RDS is very low). Fig. 10b in US Patent Application Serial No. 10/764920, included by reference, visualizes the principal RDSon characteristic versus gate voltage of the switching devices **N1-5** of a single capacitor switching stage according to **Fig. 5** By thoroughly controlling such switching device within said steady ramp-up/ramp-down or steady transition area, the capacitor in series with said switching device is effectively switched in parallel to the other capacitors with a well-controlled proportion between 0 % and 100 %. "Steady" is meant in the mathematical sense of being free of jumps or breaks. The limits of said steady ramp-up/ramp-down or steady transition area is distinguished by the points, where a further change of the controlling signal of the switch does not lead to further decrease or increase of the series resistance of said switching device (except for a small, negligible change).

In case a specific member of said switching devices is switched fully-on, the parallel connection of the capacitor (in series with said switching device in view) is fully effective (i.e. is effective to 100 %). If however a specific item of said switching devices is switched fully-off, the parallel connection of the capacitor (in series with said switching device in view) is not effective at all (i.e. is effective to 0 %). While said switching device in view is within its steady ramp-up/ramp-down or steady transition phase, the capacitor may be effectively switched in parallel with any value between 0 % and 100 %. The effectiveness of the switching in parallel of said capacitor is well controlled through the amplifiers **Amp 1** to **Amp n** and the ~~set~~ relation of tuning and reference voltages, symbolized by the voltage dividing circuit of the resistor chain **R1** to **Rn**.One can assume the steady transition area of RDS changing to be, for example, between the 2 % point and the 98 % point and define these limits as the "desired steady transition area".

The terms "steady ramp-up/ramp-down phase", "steady transition" and~~,~~ "steady transition phase" or "steady transition area" and "steady switching transition phase" will be used throughout the document to define the phase of analog switching operation (i.e. steady ramp-up/ramp-down) as opposed to a pure digital switching operation (pure on/off). The area where said steady ramp-up/ramp-down is possible, is called the "steady ramp-up/ramp-down area" or "steady transition area".~~Outside said "steady transition area" the switching device is either fully on or fully off.~~ As said before, "steady" is meant in the mathematical sense of being virtually linear, free of jumps or breaks. In the same sense, the term "continual switching" means the process of "steady ramp-up/ramp-down switching". Outside said "steady transition area" the switching device is not operating in a virtual linear mode any more, for example because it is

reaching a switching transistor's saturation. The term "outside the steady transition area" therefore defines the capacitor switching stage's operating area outside its virtually linear "steady transition area".

Therefore the switching device to switch on the capacitor, as used for the presented patent application is a "switching device with steady transition phase", in many cases shortly referenced herein as "switching device".

A detailed view on the individual ramp-up functions at the switching transistor's gate, of the circuit according to Fig. 3, is shown in **Fig. 4a**. **Vg1** to **Vg7** are the gate voltage versus tuning voltage slope of the switching stages number 1 to 7 in this example. One can assume the steady transition area of RDS changing to be, for example, between the 2 % point and the 98 % point and define these limits as the "desired steady transition area". All slopes of the individual gate voltages are strictly parallel. Threshold points **Th1** to **Th7** in **Fig. 11 4a** are equally spaced (distances **d1** to **d7** in **Fig. 4a**). **Fig. 4b** visualizes the overlapping switching operations of just 2 adjacent stages of the circuit according to Fig. 3. **Overlap** is a measure, where **Vg2** just starts to switch on stage number 2 and where **Vg1** is still in the steady transition area for stage number 1. Because said gate voltage versus tuning voltage slopes are all in parallel, all overlaps are normally the same. Selecting the distance of the threshold points **Th1** to **Thn** also determines the amount of overlap between adjacent switching stages,

Please add the following paragraph after the 1st paragraph on page 17:

A translinear amplifier typically has a gain of 1. However, a gain different from 1 is also achievable, which, if implemented, gives one more degree of freedom in dimensioning the overlapping parameters. For example, the remaining overlapping of neighboring capacitor switching stages may be even further reduced, as the slope of the steady ramp-up/ramp-down operation can be controlled with adequate selection of the gain. See the overlap of gate control voltage of two adjacent capacitor switching stages visualized as **Overlap Vg2 – Vg1** in **Fig. 4b**.

Please replace the 2nd full paragraph beginning at page 18 with the following amended paragraph:

Within a chain of said translinear amplifiers, each one can operate at a different absolute voltage level at their input and work independent at another output level. In this way the network to generate the reference voltages can be optimized independently for each stage, because the voltage level best suitable for the control operation of each switching transistor can be freely selected. In the circuit shown in **Fig. 6** as an example, the reference voltages are produced in a simple chain of resistors. The translinear amplifiers **Tr.Amp 1** to **Tr.Amp n** can adjust between said input reference voltage levels **Ref-in 1** to **Ref-in n** and the output reference levels **Ref-out-1** to **Ref-out-n**. Said translinear amplifiers then control the switching transistors **Sw 1** to **Sw n**, which in turn switch on the individual small capacitors **Cap 1** to **Cap n** in the proposed steady ramp-up/ramp-down manner. The combination of one translinear amplifier **Tr.Amp k**, combined with adequate control circuit and one switching device **Sw k** could be considered as an individual capacitor switching stage, where one of said capacitor switching stages connects to one capacitor **Cap k** out of a set of small capacitors. Each of said capacitor switching stages is controlled through the common input **Vtune** and an

individual input **Ref-in k**, All of these stages k = 1 to n have basically identical

functional characteristics.

Please replace three paragraphs, starting at the 1st full paragraph beginning at page 19
with the following three amended paragraphs:

Another key point of the invention is the implementation of a signal-limiting

functions at both ends of the steady switching transition area. As long as the switching

transistor is kept within its steady transition phase (RDS changing mode) the resistance

of the transistor linearly follows the input difference of said translinear amplifier. Once

the signal controlling the switching device leaves the desired steady transition area, the

signal condition is now changed abrupt by one of the signal limiting circuits. **Fig. 7**

visualizes this effect. The purpose is to overdrive said switching device to a fully-on

state, when said switching device is outside its desired steady transition area on the

lower resistance side and to overdrive said switching device to a fully-off status, when

said switching device is beyond its steady transition area on the higher resistance side.

Additional circuit elements, implementing said signal-limiting function, drive said

switching transistor either into deep saturation (RDSon going to 0) or drive it into its

extreme off state (RDSoff going very high) as soon as said switching device falls

outside said desired steady transition area. Such signal-limiting functions could,

according to the invention, be implemented within said translinear amplifier circuit, as it

is shown in **Fig. 7** of the referenced Patent Application US Serial No. 10/676919, filed

Oct. 1, 2003 and hereby incorporated by reference. The relevant additional signal

limiting function is presented there with the circuits **ADD-COMP 1-7 and ADD-COMP 2**.

Said signal-limiting functions could however be implemented as separate circuits

external to said translinear amplifier as well.

Fig. 7 of the instant document visualizes the idea of sharply cutting off said signal controlling the switching device as soon as ~~the~~ a changing Gate **Control Voltage Vg-7** leaves the desired steady transition area **Steady Transition Area** at the cut-off edges **CutOff Lo** and **CutOff Hi**~~, when the Tuning Voltage Vctl changes~~. For example, at the two desired points, beyond the 98 % on-point, said signal **Vg-7** controlling the switching device rises sharply and below the 2 % off n-point said signal **Vg-7** controlling the switching device is driven to rapidly switch-off. **Fig. 8** presents the same behavior as Fig. 7 for a larger number of said capacitor switching stages. **Th1** to **Thn** are the selected threshold points for said switching to occur. **d1** to **dn** are the distances of said threshold points, that normally are dimensioned to equal distance. The capactitor tuning voltage **Tuning Voltage Vctl** is supplied to all capacitor switching stages as a common signal.

Fig. 9 shows a realistic circuit diagram of an implementation, in accordance with an embodiment of this invention. **Tr.Amp 1** to **Tr.Amp n** are said translinear amplifiers, **Sw 1** to **Sw n** are the switching devices and **Cap 1** to **Cap n** are said capacitors that will be switched in parallel, resulting in the total capacitance **varCap**. **R1** to **Rn** build the resistor chain to produce references voltages for the amplifier of each stage, as already shown in Fig. 6. Similar to **Fig. 7**, the combination of one translinear amplifier **Tr.Amp k**, combined with adequate control circuit and one switching device **Sw k** could be considered as an individual capacitor switching stage, where one of said capacitor switching stages connects to one capacitor **Cap k** out of a set of small capacitors. Each of said capacitor switching stages is controlled through the common input **Vtune** and an individual input **Ref-in k**. In the implementation shown in **Fig. 9**, the reference points

Ref-out k are all connected to a common Reference point **Vref.**

All of these stages k = 1 to n have basically identical functional characteristics

Please replace the 2nd full paragraph beginning at page 21 with the following amended paragraph:

Typically, it would be desirable to achieve a linear relation between the tuning voltage and the capacitor variation, i.e. in a strictly linear mode. Then the reference voltages to compare with the tuning voltage would normally be equally spaced. However, tTo achieve a steady, but predefined non-linear relation instead, other reference voltage steps for said threshold points could also be selected, like spacing along a parabolic curve. As explained before, one circuit example is said resistor chain **R1 to Rn**, or a similar circuit, to produce a series of voltage references **Ref 1 to Ref n**, where each of said translinear amplifiers compares the tuning voltage with its dedicated reference voltage. To achieve a non-linear relation between reference points and tuning voltage, a set of reference voltages will be provided, that are, instead of being equally spaced, spaced along a desired non-linear curve. As one suggested embodiment, such non-linear relation can be achieved by appropriate selection of the values of said resistor chain **R1 to Rn.** Similar, the tuning voltage could be split into a multiple of tuning signals to feed them to the translinear amplifier inputs. Depending on the technique to implement the reference values defining said threshold points for each of the amplifiers within a chain of said translinear amplifiers-chain, specific nonlinear relations of capacitance change versus tuning voltage can be constructed. The concept of said non-linear relation is demonstrated in **Fig. 12**, with **Curve A** and **Curve B** as